Assam Hardware Testing

Overview Presentation
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Kenneth C. Barr
Contents

- Lab Configuration
- Host PC
- Host – Baseboard link
- Tester Baseboard
Lab Configuration

Custom daughtercard
PCI Development Board

Keyboard
Video
Mouse

Tower PC (dual-boot)

Tester baseboard

Power supply

ATCO on PCB

Multimeter, scope, etc.
Lab Configuration
Host PC

- Pentium III / 800 MHz
- 300 Watt Power Supply
- 440 BX Chipset
- 256-512 MB 100 MHz SDRAM
- 20G HDD, Dual Boot (Linux/Win2K)

Misc
- Vendor: PCs for Everyone
- Accessories: CDRW, PCMCIA
Host-Baseboard Link

- Development card converts PCI to a simpler local bus
- Daughtercard connects local bus to the tester baseboard
  - Provides clock
  - Line drivers and terminators
- Custom Linux driver
Tester Baseboard (Back)

From Power Supply

To/From Host

Xilinx
XC4028XL

24 MB DRAM
(holds current measurements)

16 Power Supplies
Tester Baseboard (Back)
Tester Baseboard (Front)

- **I²C**
- **JTAG Pads**
- **Clock probe connector**
- **A-D Probe pads?**
- **To/From Xilinx (Temperature)**
- **Test Chip Connectors**
- **Resets**
Tester Baseboard Features

- Xilinx XC4028XL
  - 193 User I/O pins (Max)
  - 18K-50K Gates (Typical)
  - 80MHz external, 150MHz internal

- Sixteen voltage-adjustable and current-monitored power supplies

- Controller for temperature control and measurement

- Configurable status and control bits

- Parallel 32 bit data path

- Adjustable frequency clock

- JTAG serial interface to DUTs
Adjustable Power Supplies

- Voltage adjustable between 0V-3.9V in 1 mV increments
- Current measurements stored in 24 MB DRAM
- Adjustable sample rate
  - DRAM can hold 2 seconds at 500 kSamples/s
  - DRAM can hold 64 seconds at 15 kSamples/s
Adjustable Power Supplies
Temperature Monitor/Control

- **Control**
  - Via Peltier Device
  - Estimated Accuracy: ± 2 ºC

- **Measure**
  - Range: -55 - 125 ºC
  - Error: ± 0.5 ºC

- Bond to chip in a reusable fashion

- **Documentation Issues**
  - Part numbers
  - Interface to ATC0 PCB
Control

- 32 control bits configurable on the baseboard
- Parallel bidirectional datapath between baseboard and DUT (32 bits plus control).
Clock generator frequency can be specified in 1 MHz steps from 25-400 MHz, using an external crystal as a reference.

Differential PECL outputs. Must be converted on test chip PCB to a single-ended signal with the appropriate signal levels.
ATC0 Interfaces

1. Download
2. Run Test

Or: Run same test on RTL Simulation

PC Host

Xilinx
Controller Implementation (Verilog)

Test suite (C++)

ATC0 RTL
(SyCHOSys)

Baseboard Hardware

ATC0

Test Harness

PGRAM

LARAM

DUT

Xilinx

Clock

Voltage Set/Get

Temp

Current / SDRAM