Rethink Hardware-Software Interface for Power-Aware Computing

**New Ideas:**
- Microprocessor architectures that expose energy consumption to software
- Energy-conscious compiler analyses that minimize switching activity in processors
- Simulator technology for fast accurate processor energy-performance analysis

**GOAL:** Reward compile-time knowledge with run-time energy savings

**Impact:**
- New integrated architecture and compiler techniques for power-aware systems
- Improve processor energy-delay product by 5-100x for automatically compiled code
- Fast (10-100 kHz) and accurate (<10% error) energy-performance simulation techniques for low-power microprocessors

**Schedule**

**Architecture**
- Baseline
- Single Tile
- Multi-Tile

**Energy-Performance Simulator**
- Baseline
- Single Tile
- Multi-Tile

**Compiler**
- Baseline
- Single Tile
- Multi-Tile

**Application Evaluation**
- Baseline
- Single Tile
- Multi-Tile

**MIT Laboratory for Computer Science**

Krste Asanovic, Saman Amarasinghe, Martin Rinard