Leakage-Biased Domino Circuits for Dynamic Fine-Grain Leakage Reduction

Seongmoo Heo and Krste Asanović

Massachusetts Institute of Technology
Lab for Computer Science

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Leakage Power

• Growing impact of leakage power
  – Increase of leakage power due to scaling of transistor lengths and threshold voltages
  – Power budget limits use of fast leaky transistors

• Challenge:
  – How to maintain performance scaling in face of increasing leakage power?
Leakage Reduction Techniques

Static: Design-time Selection of Slow Transistors (SSST) for non-critical paths
- Replace fast transistors with slow ones on non-critical paths
- Tradeoff between delay and leakage power

Dynamic: Run-time Deactivation of Fast Transistors (DDFT) for critical paths
- DDFT switches critical path transistors between inactive and active modes
Observation:

Critical paths dominate leakage after applying SSST techniques

Example: PowerPC 750
- 5% of transistor width is low Vt, but these account for >50% of total leakage.

⇒ DDFT could give large leakage savings
DDFT Techniques for Domino

- **Dual-$V_t$ Domino** [Kao and Chandrakasan, 2000]
  - High $V_t$ for precharge phase
  - **Input gating** $\rightarrow$ increased delay and active energy
  - High $V_t$ keeper $\rightarrow$ increased noise margin

(High $V_t$ transistor: **Green** colored)
DDFT Techniques for Domino

- **Dual-\(V_t\) Domino**
  - High \(V_t\) for precharge phase
  - Input gating \(\rightarrow\) increased delay and active energy
  - High \(V_t\) keeper \(\rightarrow\) increased noise margin
DDFT Techniques for Domino

- MHS-Domino [Allam, Anis, Elmasry, 2000]
  - Clock-delayed keeper
DDFT Techniques for Domino

- MHS-Domino
  - Pull-down through PMOS → short circuit-current in static inverter

![DDFT Techniques Diagram](image-url)
Leakage-Biased (LB) Domino

Two sleep transistors in non-critical path
Leakage-Biased (LB) Domino

Active mode

 clk

 in

 Sleep(=0)

 Sleepb(=1)
Leakage-Biased (LB) Domino

Sleep mode

LB-Domino biases itself into a low-leakage stage by its leakage current
Han-Carlson Adder

- Evaluation with carry generation
- Circuit of a 32-bit Han-Carlson adder
- 6 levels of alternating dynamic and static logic
- 4 circuits: LVT, DVT, LB, and LB2
- Constraints
  - Input/Output noise margin kept to 10% of Vdd
  - Precharge/Evaluation delay equalized to within 1% error
PG Cells of Han-Carlson Adder

(a) Low $V_t$ (LVT)

(b) Dual $V_t$ (DVT)

(c) Leakage-Biased 1 (LB)

(d) Leakage-Biased 2 (LB2)
## Processes

- **180nm**: TSMC 180nm Processes
- **70nm**: BPTM 70nm Processes

<table>
<thead>
<tr>
<th>Process</th>
<th>180nm</th>
<th>70nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>High $V_t$ (NMOS/PMOS)</td>
<td>0.46V/-0.45V</td>
<td>0.39V/-0.40V</td>
</tr>
<tr>
<td>Low $V_t$ (NMOS/PMOS)</td>
<td>0.27V/-0.23V</td>
<td>0.15V/-0.18V</td>
</tr>
<tr>
<td>$V_{dd}$</td>
<td>1.8V</td>
<td>0.9V</td>
</tr>
<tr>
<td>Temperature</td>
<td>100°C</td>
<td>100°C</td>
</tr>
</tbody>
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Input Vectors

• 3 different input vectors
  – Active energy and leakage power dependent upon inputs
  – Vec1 discharges no dynamic nodes
  – Vec2 discharges half of dynamic nodes
  – Vec3 discharges all dynamic nodes

<table>
<thead>
<tr>
<th></th>
<th>A</th>
<th>B</th>
<th>Ci</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vector 1</td>
<td>0x000000000</td>
<td>0x000000000</td>
<td>0</td>
</tr>
<tr>
<td>Vector 2</td>
<td>0xffffffff</td>
<td>0x000000000</td>
<td>0</td>
</tr>
<tr>
<td>Vector 3</td>
<td>0xffffffff</td>
<td>0xffffffff</td>
<td>1</td>
</tr>
</tbody>
</table>
Delay and Active Power: 70nm

Eval/Prech delay

Active energy

Delay (ps)

Energy (pJ)

LVT  DVT  LB  LB2

eval  prech

LVT  DVT  LB  LB2

vec1  vec2  vec3
Steady-State Leakage Power

180 nm process

Leakage power (uW)

70 nm process

Leakage power (uW)

vec1
vec2
vec3

LVT DVT LB LB2

vec1
vec2
vec3

LVT DVT LB LB2
Cumulative Sleep Energy: 180nm

vec1

vec2

vec3

Energy (pJ)

Time (us)

LVT

DVT

LB

LB2
Cumulative Sleep Energy: 70nm

vec1

vec2

vec3

Energy (pJ)

Time (ns)

LVT

DVT

LB

LB2
Conclusion

• Leakage-Biased Idea
  – *Leakage can be used to bias nodes into low-leakage states*

• LB-Domino for Fine-grain leakage reduction
  – 100x reduction in steady-state leakage
  – Low deactivation and wakeup time
  – Low transition energy
    • >10ns breakeven time at 70nm process
Acknowledgement

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